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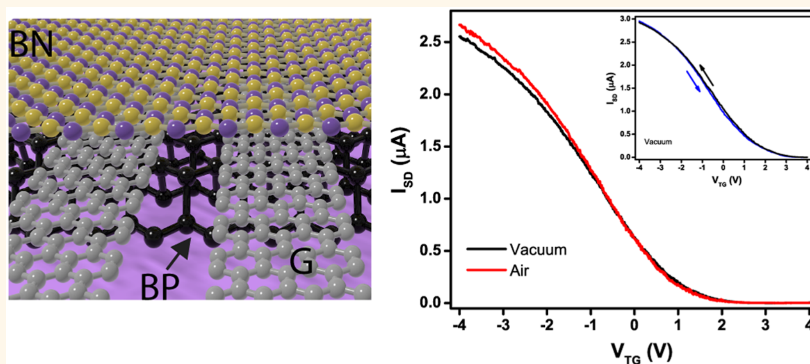
Air-Stable Transport in Graphene-Contacted, Fully Encapsulated Ultrathin Black Phosphorus-Based Field-Effect Transistors

Ahmet Avsar,[†] Ivan J. Vera-Marun,[†,‡] Jun You Tan,[†] Kenji Watanabe,[∥] Takashi Taniguchi,[∥] Antonio H. Castro Neto,[†] and Barbaros Özyilmaz*[,†,⊥]

[†]Centre for Advanced 2D Materials & Department of Physics, National University of Singapore, 2 Science Drive 3, Singapore 117542, Singapore, [‡]Physics of Nanodevices, Zernike Institute for Advanced Materials, University of Groningen, Nijenborgh 4, 9747 AG, Groningen, The Netherlands, [∥]National Institute for Materials Science, 1-1 Namiki, Tsukuba 305-0044, Japan, and [⊥]Nanocore, National University of Singapore, 4 Engineering Drive 3, Singapore 117576, Singapore

ABSTRACT



The presence of direct bandgap and high mobility in semiconductor few-layer black phosphorus offers an attractive prospect for using this material in future two-dimensional electronic devices. However, creation of barrier-free contacts which is necessary to achieve high performance in black phosphorus-based devices is challenging and currently limits their potential for applications. Here, we characterize fully encapsulated ultrathin (down to bilayer) black phosphorus field effect transistors fabricated under inert gas conditions by utilizing graphene as source—drain electrodes and boron nitride as an encapsulation layer. The observation of a linear $I_{SD}-V_{SD}$ behavior with negligible temperature dependence shows that graphene electrodes lead to barrier-free contacts, solving the issue of Schottky barrier limited transport in the technologically relevant two-terminal field-effect transistor geometry. Such one-atom-thick conformal source—drain electrodes also enable the black phosphorus surface to be sealed, to avoid rapid degradation, with the inert boron nitride encapsulating layer. This architecture, generally applicable for other sensitive two-dimensional crystals, results in air-stable, hysteresis-free transport characteristics.

KEYWORDS: black phosphorus · graphene electrode · work function · Schottky barrier · ohmic contact · boron nitride encapsulation · hysteresis

Monolayer black phosphorus (BP) or phopshorene, a one-atom-thick sheet of phosphorus atoms arranged in a puckered structure, has recently emerged as a potential candidate to address the shortcomings of previously studied 2D materials.[1−4] Few-layer BP can be easily cleaved from bulk crystals due to weak interlayer van der Waals interactions. Its transport properties depend strongly on the thickness of the obtained crystals, and it has a direct band gap, increasing monotonically from ~0.3 eV in bulk to ~1.7 eV in phosphorene.[5] These properties, together with recent observations of high mobilities up to 1000 cm^2/V·s[1,3,4] at room temperature (1 order of magnitude higher than previous semiconducting 2Ds[6]) make BP suitable for applications such as fast and broadband photodetectors,[7] solar cells,[8] and digital electronics.[1]

* Address correspondence to barbaros@nus.edu.sg.

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Field-effect transistors (FET) consist of an active semiconductor where charge carriers flow between source and drain electrodes and an electrostatic gate modulating the carrier density in the channel. For practical applications, the source and drain electrodes are expected to exhibit low contact resistances and linear response, while the semiconducting channel should be stable over time. FETs using BP channel have already exhibited high on/off ratio,[1,2,4,9] low subthreshold swing,[1,10] and excellent current saturation[1,4] making BP attractive for semiconductor device applications. However, the preparation of BP-based devices still poses challenges. The BP channel tends to degrade after a short exposure to air due to a photoactivated charge transfer process.[11] This degradation not only increases the surface roughness but also leads to the formation of chemisorped species. In particular at the contacts, these species cause metal-induced gap states due to strongly hybridization and, hence, result in large Schottky barrier heights.[12] Therefore, such interfaces have large contact resistances and a highly nonlinear response and pose a major problem in optimizing device performance.

RESULTS AND DISCUSSION

In this work, we offer a solution to these contact and stability problems of BP FETs by creating a 2D heterostructure where all interfaces are based on van der Waals bonding.[13] Toward this end, we have contacted atomically thin layers of BP (purchased from Smart Elements) with monolayer graphene and fully encapsulated the device with hexagonal boron nitride (h-BN) in a layer-by-layer fashion, all under an inert argon environment with minimized water and oxygen content. Using graphene electrodes in our device device architecture solves two key issues. First, the integration of graphene electrodes with a tunable work function[14] lowers the contact resistance. The observation of a linear $I_{SD}-V_{SD}$ characteristic down to 10 K indicates that ohmic contacts are indeed achieved. Second, graphene allows ultrathin h-BN crystals to fully conform to the underlying structure without leaving any space for air or other species to diffuse. Such an encapsulation leads to the observation of equally good performances under both ambient and vacuum conditions in our heterostructures. Our results are important toward fabrication of high quality BP devices relevant for operation under ambient conditions.

The device fabrication starts with the etching of mechanically exfoliated monolayer graphene flakes into isolated contact stripes by using standard electron beam lithography and oxygen plasma techniques. Few layers of h-BN crystal are partially deposited onto these monolayer graphene stripes with a dry-transfer method.[15,16] The graphene/h-BN stack is isolated from the wafer with a KOH etching process. Meanwhile, a thin BP crystal is exfoliated onto the SiO_2 (300 nm)/Si wafer in a glovebox (argon environment), followed by the transfer of the graphene/h-BN stack onto this freshly exfoliated BP crystal. We take care that h-BN fully encapsulates the BP crystal. During the device fabrication process, the surface of BP has never been exposed to air. Fabrication is completed with forming Cr/Au (2 nm/80 nm) electrodes on nonencapsulated regions of the graphene stripes and on top of the h-BN crystal. These serve as source–drain electrodes and top gate electrodes, respectively. We note that our device architecture protects BP from both possible electron beam lithography and metal deposition damages. A more detailed description of the device fabrication is discussed in the Supporting Information.

Optical images of the device before and after the metallization process are shown in parts a and b, respectively, of Figure 1. The final device is annealed at 340 °C under high vacuum conditions. This annealing step is crucial to obtain high-quality contacts. First, the annealing treatment improves the bonding of graphene and h-BN layers to the BP crystal by removing the small bubbles that might be formed during the transfer process.[15] Second, it removes the possible adsorbants present at the interface of BP and SiO_2 that can cause significant hysteresis in transport measurements.[17] AFM images confirm that the device is clean and free of wrinkles (Figure 1c). The resulting heterostructure is illustrated schematically in Figure 1f. A Raman spectrum for the encapsulated BP device is shown in Figure 1d where the characteristic[18] A_g^1, B_{2g}, and A_g^2 peaks of BP are clearly visible at the wave numbers of 362.6, 439.8, and 467.4, respectively. We do not observe any obvious change in the Raman spectrum before and after annealing at 340 °C, implying that the encapsulating h-BN crystal effectively protects BP. It is worth noting that nonencapsulated BP crystals degrade under identical annealing processes (see the Supporting Information). Electronic transport measurements are carried out in a two-terminal configuration under both ambient and vacuum conditions ($\sim 1 \times 10^{-7}$ Torr). In this work, we studied a total of three samples and present representative data on two encapsulated BP devices with thicknesses of ~4.5 nm (6 layer, sample S1) and ~1.6 nm (2 layer, sample S2), respectively. Unless otherwise stated, the results obtained in the relatively thicker sample are discussed in the manuscript. SiO_2 (~300 nm) and h-BN (~16 nm) dielectrics are utilized to apply back and top gate biases (V_{BG} and V_{TG}), respectively (see Figure 1e). The bias current (I_{SD}) of BP-based devices is characterized as a function of source–drain voltage (V_{SD}), temperature (T), V_{BG}, and V_{TG}.

First, we discuss the graphene contact aspect of our manuscript. Parts a–c of Figure 2 show the 2D color plots of I_{SD} as a function of V_{SD} and V_{BG} at $V_{TG} = -4$, 0, 4 V, respectively. The measurements are carried out at room temperature. The device shows p-type behavior

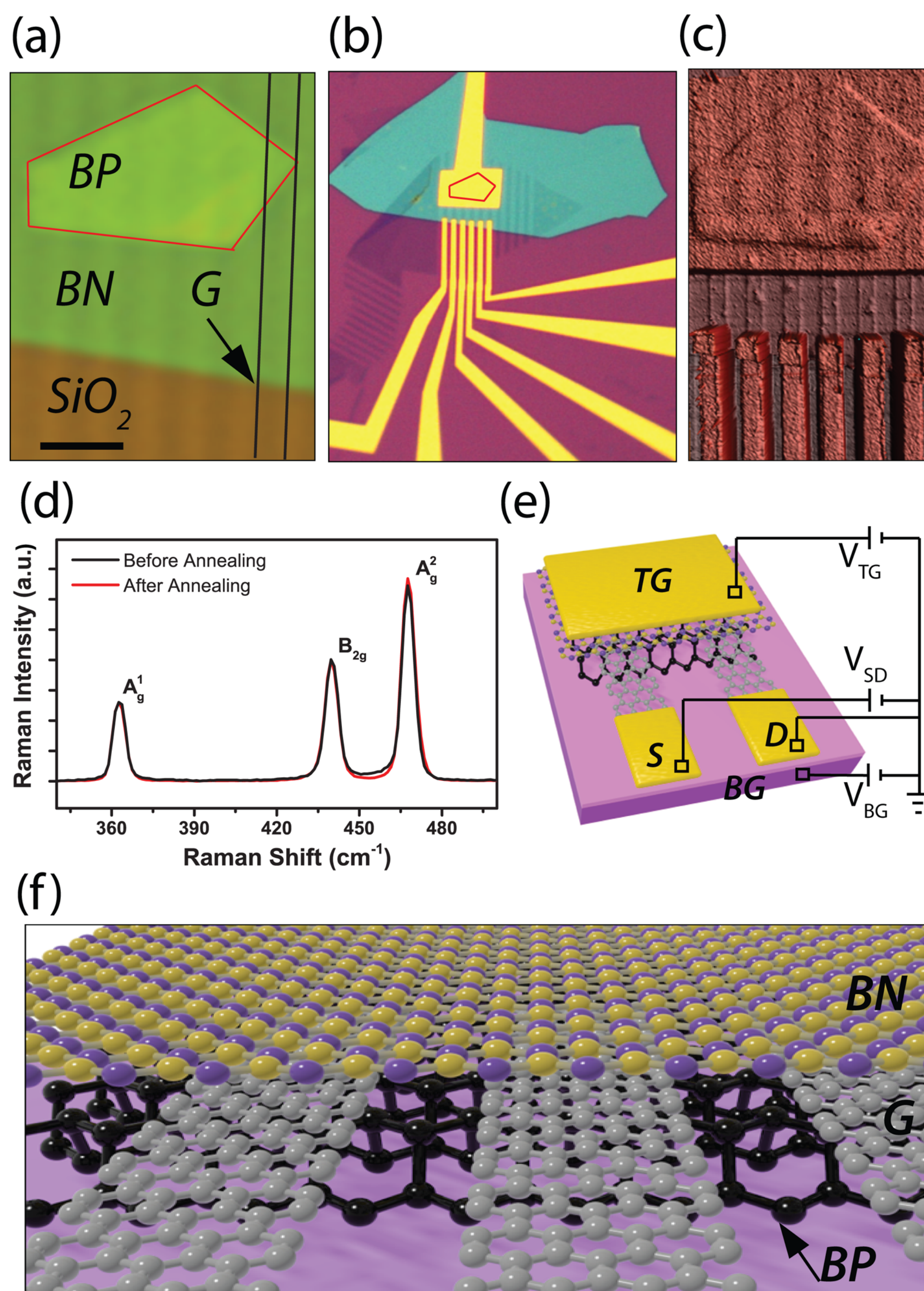

Figure 1. Device fabrication and characterization. (a) Optical image of the device after the final transfer process. Red and black areas show the black phosphorus crystal and one of the graphene stripes, respectively. (b) Optical image of the device after the contacts are formed. (c) Atomic force microscopy image of the device after the final annealing step. Height color is 50 nm. (d) Raman spectroscopy of few layers of encapsulated black phosphorus flake before and after annealing process. (e) The schematics of graphene contacted BP device together with the electrical connections for the device characterization. (f) The schematics of the atomically sharp interfaces in encapsulated BP device. The black, gray, blue, and yellow spheres represent the phosphorus, carbon, boron, and nitrogen atoms, respectively.

even at $V_{TG} = 4$ V. The application of V_{TG} causes a clear shift in the threshold region which starts to be observed at more positive V_{BG} values. However, I_{SD} still shows a saturation behavior at high negative V_{BG} values independent of V_{TG}. To elucidate this behavior, we plotted the V_{BG} dependence of I_{SD} at $V_{SD} = 0.1$ V for $V_{TG} = -4, 0, 4$ V (Figure 2d). While we see saturation behavior for each values of V_{TG}, remarkably, the magnitude of the saturation current increases as the V_{TG} is decreased. It has been extensively discussed that the saturation current in 2D semiconductor-based FETs is dominated by the contact resistance in a two-terminal FET structure.[4,19,20] Therefore, the observation of the increase in the saturation current as the V_{TG} decreases indicates that contact quality is improved. To quantify this, the total resistance *vs* V_{BG} curve is

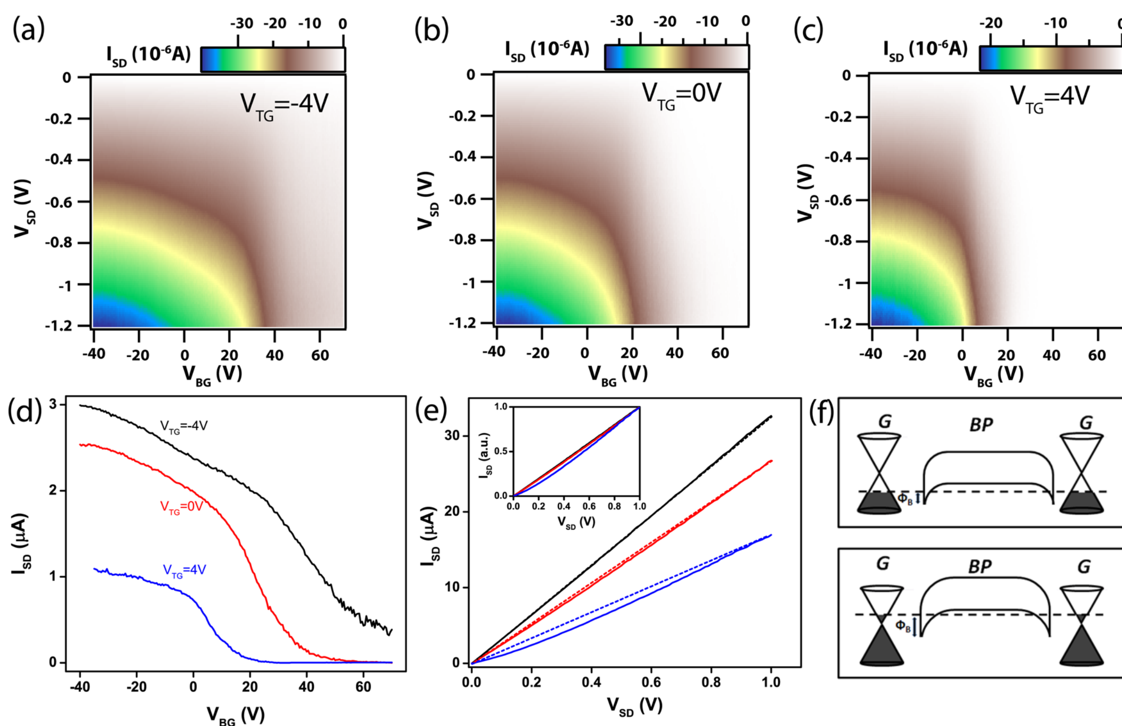

Figure 2. Device performance of black phosphorus device utilizing graphene electrodes (a–c) 2D color fan plot of bias current as a function of back gate and source–drain biases at fixed top gate voltage values of −4, 0, 4 V, respectively. (d) Back gate voltage dependence of bias current at different top gate voltage values. (e) Source–drain voltage dependence of bias current at different displacement fields. Black, red, and blue lines represent V_{TG} = −4, 0, and 4 V, while V_{BG} is fixed to −30 V. Inset shows the renormalized values of(e) for more clarity. All measurements are performed on a ∼4.5 nm thick sample at room temperature. (f) Top and bottom schematics illustrate the band alignments for the V_{TG} = −4 and 4 V at fixed V_{BG} = −30 V cases, respectively.

extrapolated as suggested by Roy *et al.* by using the polynomial $(A) + (B/x) + (C/x^2)$ where the fitting parameter A refers to the contribution of the contact resistance to the total device resistance at very high gate biases where the resistance of BP channel is substantially small. The fitting parameters B and C on the other hand describe mainly the resistance of the graphene and BP channels itself.[19] We observe a sharp decrease in the magnitude of the contact resistance (resistivity) from ∼41.5 kΩ (38.2 kΩ.μm) to ∼11.2 kΩ (10.3 kΩ.μm) by only changing the V_{TG} from 4 to −4 V (see the Supporting Information for details). Here, we also find that the resistance of the black phosphorus channels is only ∼3.7% of the total device resistance at the saturation region. We note that these extracted contact resistances are upper bound estimations, since the metal leads, the graphene/metal interfaces, and the graphene channels have additional Ohmic contributions in series to the total contact resistance. We believe that similar to earlier work on MoS_2,[19] the larger than expected series resistance of our contacts is caused by the annealing conditions needed to form a low barrier interface between graphene and BP. It is well-known that the resistance of graphene on SiO_2 increases when 300 °C is exceeded during annealing.[21] In future experiments, this problem can be avoided by replacing the rough SiO_2 substrate with a flat BN substrate as has been already demonstrated elsewhere for graphene on BN devices.[22,23]

The observation of such an improvement in contact resistance upon tuning the vertical electric field is due to the unique work-function tunability of graphene electrodes. This allows for a higher efficiency of hole injection to the valence band of BP at high electric fields.[14] As schematically shown in Figure 2f, the application of large negative gate voltages (both V_{TG} and V_{BG} are negative) shifts the Fermi level of graphene toward the valence band of BP. This creates better band matching between graphene and BP by bending the conduction and valence bands upward. Therefore, at high electric fields it is easier to inject holes from graphene source–drain electrodes to BP. The Fermi level of graphene electrodes on top of BP is primarily tuned by V_{TG} rather than V_{BG} in our device. Note that, Li *et al.* have shown that the charge-screening length of the BP crystal is ∼2.9 nm.[1] Therefore, V_{BG} is not expected to strongly tune the graphene Fermi level in our 4.5 nm thick sample. Instead, the Fermi level is mainly determined by V_{TG}.

The relation between I_{SD} and V_{SD} provides further information about the nature of contacts. Therefore, we study the relation between I_{SD}–V_{SD} at different gating conditions. As shown in Figure 2e, I_{SD}–V_{SD} deviates from linearity at large displacement fields

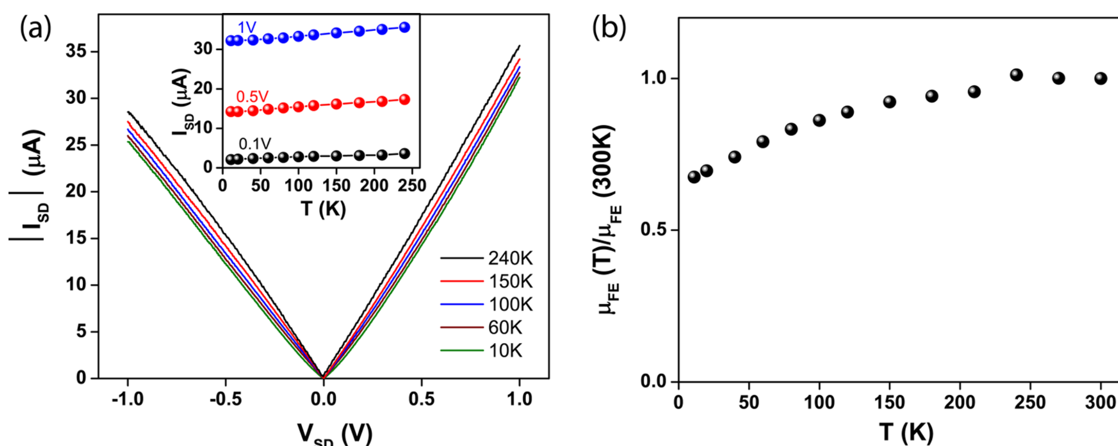

Figure 3. Temperature-dependent characterization of black phosphorus device utilizing graphene electrodes (a) Source–drain bias voltage and temperature dependence of bias current at fixed top gate (−4 V) and back gate (−70 V) voltage. Inset shows the temperature dependence of bias current at different source-bias voltage values. (b) Temperature dependence of two-terminal field effect mobility for the ∼4.5 nm thick sample.

(V_{TG} = 4 V, V_{BG} = −30 V). However, it becomes more linear as V_{TG} is swept to 0 V, and eventually, we observe a perfectly linear relation upon the application of smaller displacement fields (V_{TG} = −4 V, V_{BG} = −30 V). Such a linear behavior indicates that our contacts become ohmic[24] as V_{TG} is tuned due to the gate modulation of the graphene workfunction. It is also worth noting that both encapsulated and nonencapsulated BP devices with Ti/Au contacts have nonlinear $I_{SD}-V_{SD}$ behavior in all gating conditions in sharp contrast to this graphene-contacted device (see the Supporting Information).

Next, we carried out a detailed study of I_{SD} as a function of temperature in order to confirm the ohmic nature of our contacts. Figure 3a shows the V_{SD} and T dependence of I_{SD} at V_{BG}= −70 V and V_{TG} = −4 V. We observe a linear relationship between I_{SD} and V_{SD} at both current polarities for all temperatures. Remarkably, the change in I_{SD} is less than 10% within the temperature range of 300 to 10 K. However, in order to unambiguously exclude the presence of a Schottky barrier, we analyze the data using the termionic emission model describing the charge transport through a schottky barrier into the BP channel

$$I_{SD} = AA^*T^{1.5}\exp\left[-\frac{e}{k_BT}\left(\Phi_B - \frac{V_{SD}}{n}\right)\right]$$

where A is the contact area, A^* is the 2D Richardson constant, e is the electron charge, k_B is the Boltzmann constant, and Φ_B is the Schottky barrier height and n is the ideality factor.[25] We find that Schottky barrier height values are very small. In fact, extracted values are found to be negative, ranging from −17 to −2.5 meV in all gating conditions (see the Supporting Information). This proves that thermionic emission is not the dominant transport mechanism in these graphene-contacted BP devices. In contrast to a recent report on a metal-contacted BP device[10] that has charge injection dominated by thermionic emission, the nearly temperature insensitivity of I_{SD} in our graphene-contacted device suggests that charge injection is ohmic.

The weak temperature dependence of our contacts should have minimal impact on the transport in two terminal BP-based FETs where (unlike the four-terminal geometry) contacts play an important role.[4] Figure 3b shows the temperature dependence of the field effect mobility, normalized to the rt value ($\mu_{FE}(T)/\mu_{FE}$ (300 K) where μ_{FE}(300 K) = 63 cm^2/V·s). The device demonstrates remarkable temperature stability; a negligible decrease of mobility from rt down to 100 K (∼10%) and only a moderate decrease down to 10 K (∼30%) is observed. A previous report on a Ti/Au-contacted BP device[4] has shown a decrease in mobility of more than 80% in a two-terminal measurement configuration as the temperature is reduced from rt to 20 K. Such significant improvement in our device is due to the absence Schottky barrier heights at the both source and drain graphene electrodes. However, we note that in the two-terminal geometry even reduced contact barrier has significant influence on the device characteristics.[4] Here, the extracted mobility underestimates the intrinsic mobility and is most likely responsible for its decreasing behavior with decreasing temperature.[26]

Now we turn our attention to the equally important stability aspect of our device. We study the transport characteristics of our encapsulated device by measuring under both vacuum and ambient conditions. For comparison, we also fabricated a nonencapsulated device with similar thickness of BP crystal (insets of Figure 4a,b). Figure 4a shows the V_{TG} dependence of I_{SD} at fixed V_{BG} (−40 V) and V_{SD} (100 meV) under vacuum conditions. While the nonencapsulated device shows a significant hysteresis (∼30 V) even under

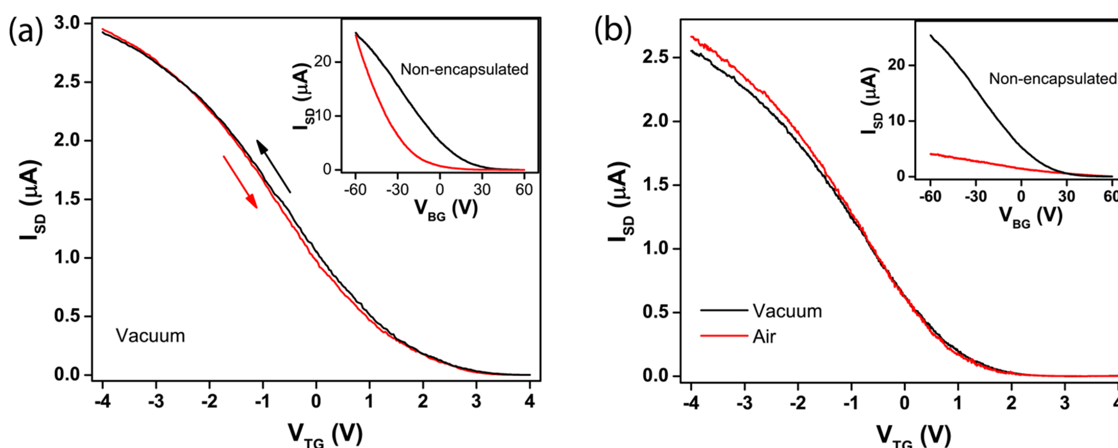

Figure 4. Device stability of fully encapsulated black phosphorus device. (a) Top gate voltage dependence of bias current in encapsulated device at fixed back gate (−40 V) and source−drain (100 meV) biases. Black and red arrows represent the forward and backward gate sweeps, respectively. The inset shows the transport curve of a nonencapsulated device. The hysteresis is caused by a charge-transfer process (positive hysteresis). Black and red lines represent the forward and backward gate sweeps, respectively. (b) Top gate voltage dependence of bias current under vacuum (black line) and ambient conditions (red line) at fixed back gate (0 V) and source−drain (100 meV) biases. The inset shows the gate voltage dependence of a nonencapsulated device. All measurements are performed in ∼4.5 nm thick sample at room temperature.

vacuum conditions, the encapsulated device has nearly hysteresis-free transport characteristics. In general, such positive hysteresis is caused by both the sensitivity of 2D crystals to the external chemical environments and with the hosting substrate (see the Supporting Information).[17,27] In our device, the first is excluded as the device is fully encapsulated. The second potential source is also eliminated due to the high-temperature annealing treatment during device fabrication. In fact, our architecture is so robust that even after 2 months the gate sweeps show negligible hysteresis (see the Supporting Information, section 5). Next, we discuss the transport performance under ambient conditions. As can be seen in Figure 4b, the encapsulated device has nearly identical output characteristics under both ambient and vacuum conditions. On the other hand, for the nonencapsulated device we observe a significant drop in the conductivity (up to 80%) at ambient conditions (Figure 4b inset), resulting in lower field effect mobility and current modulation (see the Supporting Information). These observations clearly indicate that the high-quality h-BN encapsulating layer together with monolayer graphene electrodes protect the BP surface from interaction with air. It is worth noting that utilizing metal contacts rather than monolayer graphene does not allow a full sealing even when encapsulated with the h-BN layer and results in significant hysteretic behavior (see the Supporting Information). Also, compared to other passivation schemes such as SiO_2-, PMMA-, and ALD-grown dielectrics of Al_2O_3 and HfO_2, h-BN is intrinsically inert and pinhole free.[23,28] This minimizes the possible oxidation of BP through pinholes in the dielectric and avoids potential chemical reactions. For example, the water pecursor in ALD grown Al_2O_3 was shown to cause hysteresis in MoS_2-based FETs.[27,29] Such an effect will be more dramatic in BP-based devices as the crystal is very sensitive to the adsorbed oxygen in water.[30] In contrast, in our heterostructure device the interfaces remain pristine as demonstrated by the lack of hysteresis and the stability discussed above.

Finally, we remark that our device architecture allows us to study very thin layers of BP, which is otherwise very challenging due to the issue of its rapid degradation. The recent prediction of band gap modulation in a dual-gated bilayer BP device[8] makes our approach attractive for the perpective of fundamental science as well. Toward this, we utilized our encapsulated device architecture to study the transport properties of a bilayer BP-FET device. Figure 5 shows the V_{BG} dependence of I_{SD} at fixed V_{SD} = 0.1 V. Similar to the previously shown device, bilayer BP-based FET also shows a dominant p-type behavior. However, we achieve a clear bipolar behavior where both electron and hole conduction are observed. This result is consistent with a strongly reduced electric field screening in such ultrathin samples.[31] In this device, we observe at room temperature an on/off ratio of ∼100 and a subthreshold swing of ∼30 V and ∼17 V per decade at the hole and the electron conduction side, respectively. The observation of a smaller on/off ratio in bilayer BP compared to thicker crystals is surprising and is mainly due to the presence of a high "off" current. In our opinion, this could be related to our high temperature-annealing step during device fabrication. Thinner BP crystals have been shown to start decomposing at smaller temperatures (∼400 °C) compared to thicker crystals (∼550 °C).[32] Hence, our high-temperature annealing step could also lead to defects in our crystal which could give rise to higher "off" currents due to hopping transport.[33] Since the onset

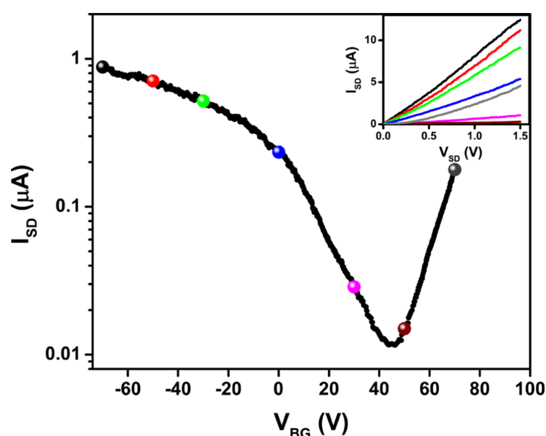

Figure 5. Device performance of bilayer-black phosphorus device utilizing graphene electrodes. Back gate voltage dependence of bias current in a bilayer BP-based device at fixed source−drain voltages (0.1 V). Inset shows the source−drain voltage dependence of bias current at fixed back gate voltage values. All measurements are performed at room temperature under vacuum conditions.

temperature for defect formation is thickness dependent, this challenge could be addressed in future experiments by carefully fine-tuning the annealing temperature with respect to the layer number in the BP device. On the other hand, the subthreshold swing value is comparable to the previous results obtained with similar SiO_2 dielectric thicknesses;[1,10] however, we note that the thicker samples show smaller subthreshold swing values (see the Supporting Information). Similar to the thicker device, we achieve a linear $I_{SD}-V_{SD}$ relation but only at the p-type region as shown in the inset of Figure 5. This linear relation is not observed in the n-type region. One potential reason for this behavior is the larger band gap in bilayer BP when compared to the thicker crystal. Here, the tuning of the Fermi level of graphene with only V_{BG} could be insufficient to enable a perfect band matching between graphene and the conduction band of BP. In fact, this interpretation seems to be in a good agreement with a recent study where ohmic (Schottky) graphene/bilayer BP interfaces were predicted upon the application of negative (positive) gate voltages.[34] Next, we calculated the field effect mobilities of this encapsulated bilayer BP device. Mobilities of ∼120 $cm^2/V\cdot s$ at the hole side and ∼40 $cm^2/V\cdot s$ at the electron side are extracted by using[1,2,4]

$$\mu = \frac{L}{W}\frac{1}{C_{OX}}\frac{1}{V_{SD}}\frac{\partial I_{SD}}{\partial V_{SD}}$$

Here, μ is the field effect mobility, L and W are the length and width of the measured junction, respectively, and $C_{OX} = \varepsilon\varepsilon_{OX}/d$ is the capacitance of SiO_2 substrate. We note that unlike previously studied semiconducting 2D crystals,[35,36] the encapsulation and enhanced graphene contacts do not improve the mobility of the encapsulated devices compared to nonencapsulated devices significantly. This suggests that the mobility is limited either by the SiO_2 substrate[1,4] or impurities in the crystal[37] rather than the adsorbants present due to air exposure and high Schottky barrier heights.

CONCLUSIONS

In conclusion, we report the fabrication of a new device architecture that allows charge-transport studies in ultrathin BP crystals reliably by utilizing monolayer graphene and ultrathin h-BN as source−drain contacts and encapsulating layer. Utilizing work-function tunable graphene electrodes into our heterostructure eliminates the Schottky barrier height, with current injection occurring through the transparent interface. We further demonstrate that these devices are extremely robust to the environment, and hysteresis is nearly eliminated due to the effective encapsulation. Our findings provide an important step toward fundamental and applied studies in phosphorene-based FET as well as give access to study the transport properties of other sensitive crystals such as silicine[38] and GaSe.[22]

Conflict of Interest: The authors declare no competing financial interest.

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Supporting Information Available: Details of fabrication process flow, effect of annealing on the stability of nonencapsulated black phosphorus crystals, hysteresis in nonencapsulated devices, charge transport in a nonencapsulated device at low temperature, robust transport in encapsulated device, additional hysteresis data, encapsulated devices contacted with Ti/Au contacts, discussion on the contribution of thermionic emission for the charge injection, work function tunability of graphene electrodes, current modulation and subthreshold swing in encapsulated device, temperature-dependent gate sweep of bias current in encapsulated device, and contact resistance extraction. This material is free of charge *via* the Internet at http://pubs.acs.org.

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